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(54) CLOCK GENERATION SYSTEMS AND **METHODS**

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(57)**ABSTRACT**

A low power reconfigurable processor core includes one or more processing units, each unit having a clock input that controls the performance of the unit; a wireless transceiver transmitting and receiving at a frequency based on a wireless clock input; and a controller having a plurality of clock outputs each coupled to the clock inputs of the processing units and the wireless clock input, the clock outputs being generated from a common master clock.

